Electronic Version
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Claims

[c1] 1. A method of fabricating a non-volatile memory device, comprising the steps of:
providing a substrate;
forming a trench in the substrate;
forming a bottom oxide layer on the substrate and the surface of the trench;
forming a charge-trapping layer over the bottom oxide layer;
forming a top oxide layer over the charge-trapping layer;
forming a conductive layer over the top oxide layer and filling the trench;
patterning the conductive layer to form a gate over the trench;
removing the top oxide layer, the charge-trapping layer and the bottom oxide layer outside the gate; and
forming source/drain regions besides the gate by performing a doping process.

[c2] 2. The method of claim 1, wherein before forming the trench in the substrate, the method further comprises a step of isolating active regions on the substrate.

[c3] 3. The method of claim 1, wherein the step of forming

the bottom oxide layer on the substrate and the surface of the trench comprises performing a thermal oxidation process to form the bottom oxide layer.

[c4] 4. The method of claim 1, wherein the step of forming the charge-trapping layer over the bottom oxide layer comprises performing a chemical vapor deposition process to form a silicon nitride layer as the charge-trapping layer.

[c5] 5. The method of claim 1, wherein before forming the source/drain regions, the method further comprises:
performing a light doping process; and
forming spacers on the sidewalls of the gate.

[c6] 6. The method of claim 1, wherein the gate extends to the substrate surface outside the trench.

[c7] 7. The method of claim 1, wherein the method comprises a step of performing a self-aligned silicide process to form a silicide layer over the gate surface.

[c8] 8. The method of claim 7, wherein before performing the self-aligned silicide process, the method further comprises forming a self-aligned metal silicide blocking layer over a portion of the substrate.

[c9] 9. A non-volatile memory device, comprising:

a substrate, wherein the substrate has a trench;
a gate disposed over and completely filling the trench;
a bottom oxide layer disposed between the gate and the trench surface;
a charge-trapping layer disposed between the gate and the bottom oxide layer;
a top oxide layer disposed between the gate and the charge-trapping layer; and
a plurality of source/drain regions configured in the substrate outside the gate.

[c10] 10. The non-volatile memory device of claim 9, wherein the gate extends over a portion of the substrate outside the trench.

[c11] 11. The non-volatile memory device of claim 10, wherein bottom oxide layer is disposed between the gate and the substrate.

[c12] 12. The non-volatile memory device of claim 9, wherein the device further comprises a plurality of spacers located on the sidewalls of the gate.

[c13] 13. The non-volatile memory device of claim 12, wherein the device further comprises a plurality of lightly doped regions located in the substrate underneath the spacers.

[c14] 14. The non-volatile memory device of claim 12, wherein

material constituting the spacers comprises silicon nitride.

[c15] 15. The non-volatile memory device of claim 9, wherein material constituting the gate comprises polysilicon.

[c16] 16. The non-volatile memory device of claim 9, wherein material constituting the charge-trapping layer is selected from the group consisting of a nitride compound, tantalum oxide, titanic strontium and hafnium oxide.

[c17] 17. The non-volatile memory device of claim 9, wherein the device further comprises a silicide layer disposed on the gate surface.

[c18] 18. The non-volatile memory device of claim 17, wherein material constituting the metal silicide layer is selected from the group consisting of cobalt silicide, titanium silicide, tungsten silicide, molybdenum silicide, platinum silicide and nickel silicide.